Claims

What is claimed is:

1. A system for modeling a hardware design for carrying out an operation wherein the hardware design includes:

an integrated circuit having a processor and an internal bus;

a hardware model containing the integrated circuit;

a bus functional model employing a first system interface unit and a second system interface unit;

means for disabling the processor of the integrated circuit;

means for simulating the operation of the processor; and

means for modeling the internal bus of the integrated circuit and providing signals which would ordinarily appear on the internal bus of the hardware design.

2. The system of claim 1 wherein the integrated circuit is a microcontroller.

3. The system of claim 2 wherein the microcontroller is a Motorola MPC860.

4. The system of claim 1 wherein the first system interface unit of the bus functional model communicates over an external bus to the hardware design, and the second system interface unit of the bus functional model communicates with the hardware model.

5. The system of claim 1 wherein the means for disabling the processor of the hardware model requires the core of the processor to not issue any bus cycles.

6. The system of claim 5 wherein disabling the processor is accomplished by using initialization code to put the processor into an endless loop.

7. The system of claim 6 whereby the endless loop is accomplished by programming the processor to execute out of Cache forever until the processor receives interrupts.

8. The system of claim 1 wherein the means for simulating the operation of the processor is accomplished such that the functional behavior of the system is provided through a combination of hardware and software.

9. The system according to claim 8 wherein at least some of the software-provided functional behavior is provided by an instruction set simulator.

10. The system according to claim 8 wherein at least some of the software-provided functional behavior is provided by the bus functional model.

11. A hardware model containing the integrated circuit having a processor and internal bus, including:

means for disabling the processor;

means for allowing a direct communication between the bus functional model and the hardware model to send interrupt service routines without passing through the processor.

12. The system of claim 11 wherein the integrated circuit is a microcontroller.

13. The system of claim 12 wherein the microcontroller is a Motorola MPC860.

14. The system of claim 11 wherein the means for disabling the processor of the hardware model requires the core of the processor to not execute any code.

15. The system of claim 14 wherein disabling the processor is accomplished by using initialization code to put the processor into an endless loop.

16. The system of claim 15 whereby the endless loop is accomplished by programming the processor to execute out of Cache forever until the processor receives interrupts.

17. The hardware model of claim 11 wherein the internal bus of the integrated circuit may be temporarily uncoupled from the hardware design so that initialization of the operating system only communicates with the instruction set simulator.

18. A system for modeling a hardware design for carrying out an operation wherein the hardware design includes an integrated circuit having a processor and an internal bus; the system comprising:

a simulator circuit simulating the hardware design and including the integrated circuit;

an instruction set simulator for representing an operation of the processor; and

means for disabling the processor.

19. A system for modeling a hardware design according to claim 18 wherein the simulator circuit comprises:

a hardware model containing the integrated circuit having the processor and the internal bus;

a bus functional model for interfacing the instruction set simulator to the simulator circuit wherein the simulator circuit can carry out the operation without intervention of the processor for determining whether the hardware design is correct; and

a transfer memory to pass system interrupts between the hardware model and the bus functional model.

20. The system for modeling a hardware design according to claim 19 wherein the hardware model simulates the integrated circuit by communicating with the bus functional model through a system interface unit.

21. The system for modeling a hardware design according to claim 18 wherein the instruction set simulator is external to the simulator circuit and executes interrupt service routines.

22. A hardware model containing the integrated circuit having the processor and the internal bus, including:

means for disabling the processor;

means for allowing a direct communication between the bus functional model and the hardware model to send interrupt service routines without passing through the processor.

23. The hardware model of claim 22 wherein the internal bus of the integrated circuit may be temporarily uncoupled from the hardware design so that initialization of the operating system only communicates with the instruction set simulator.

24. A method of modeling an integrated circuit, comprising the following steps:

putting a central processing unit (CPU) into an inactive state;

servicing an instruction set simulator (ISS) access into peripheral devices;

servicing peripheral-generated cycles; and

servicing peripheral-generated interrupt requests.

25. The method of claim 24, wherein the steps are performed independently of each other.

26. The method of claim 24, wherein the steps are performed in any order or simultaneously.

27. The method of claim 24, wherein the integrated circuit is a microcontroller.

28. The method of claim 25, wherein the microcontroller is a Motorola MPC 860.

29. The method of modeling the integrated circuit of claim 24, wherein the peripheral devices are communication processor module (CPM).